(AF)

0057-2533-2YY CONT

#11/C
T. Bell
1.9.02

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

HIDEKI TAKAHASHI : EXAMINER: LOKE, S.

J.S
2-1-02

SERIAL NO: 09/421,217 :

FILED: OCTOBER 20, 1999 : GROUP ART UNIT: 2811

FOR: INSULATED GATE SEMICONDUCTOR DEVICE WITH LOW ON VOLTAGE AND MANUFACTURING METHOD THEREOF

RESPONSE

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Office Action of October 10, 2001, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend Claim 22 as follows:

figs. 3, 22, 23

22. (Twice Amended) An insulated gate semiconductor device, comprising:

a first semiconductor layer of a first conductivity type having first and second main surfaces on opposite sides thereof;

a second semiconductor layer of a second conductivity type provided on said first main surface of said first semiconductor layer;